WHAT IS CLAIMED IS:

1. A microcomputer comprising:

a CPU;

a watch-dog timer for outputting an abnormality detection signal when a clear signal input from the CPU stops over a predetermined supervisory time;

a sleep control timer for outputting a recovery command signal for recovering the CPU to a normal operation mode when a predetermined recovery time passes after the CPU changes to a low power-consumption mode;

a common counter for counting an operation clock inputted in both the low power-consumption mode and the normal operation mode, a count value of the common counter being cleared based on the clear signal input;

a supervisory time register for holding a count setting value of the operation clock according to the predetermined supervisory time;

a recovery time register for holding a count setting value of the operation clock according to the predetermined recovery time;

a supervisory comparing means which is activated in the normal operation mode and outputs the abnormality detection signal based on a result of comparison between the count value of the common counter and the count setting value of the supervisory time register; and

a recovery comparing means which is activated in the low power-consumption mode and outputs the recovery command signal

based on a result of comparison between the count value of the common counter and the count setting value of the recovery time register.

2. The microcomputer according to claim 1, wherein:

the supervisory comparing means includes a supervisory comparator for comparing the count value of the common counter and the count setting value of the supervisory time register, and a supervisory gate means for passing an output signal of the supervisory comparator therethrough in the normal operation mode; and

the recovery comparing means includes a recovery comparator for comparing the count value of the common counter and the count setting value of the recovery time register, and a recovery gate means for passing an output signal of the recovery comparator therethrough in the low power-consumption mode.

3. The microcomputer according to claim 1, wherein:

the supervisory comparing means includes a supervisory gate means for passing the count value of the common counter therethrough in the normal operation mode, and a supervisory comparator for comparing an output value of the supervisory gate means and the count setting value of the supervisory time register; and

the recovery comparing means includes a recovery gate means for passing the count value of the common counter therethrough in the low power-consumption mode, and a recovery comparator for comparing the output value of the recovery gate means and the count

setting value of the recovery time register.

4. The microcomputer according to claim 1, wherein the recovery time register holds a count setting value which is a sum of the count value of the common counter when a CPU mode changes from the normal operation mode to the low power-consumption mode and the count value of the operation clock corresponding to the predetermined recovery time.

5. The microcomputer according to claim 1, wherein the common counter is cleared when a CPU mode changes from the normal operation mode to the low power-consumption mode and the recovery time register holds the count value of the operation clock corresponding to the predetermined recovery time.

6. The microcomputer according to claim 1, wherein the recovery command signal for recovering from the low power-consumption mode to the normal operation mode is outputted when a predetermined recovery condition occurs in addition to passing of the recovery time.

7. The microcomputer according to claim 6, wherein the predetermined recovery condition is an input of the recovery command signal from the outside of the microcomputer.

8. The microcomputer according to claim 1, wherein a buffer register is provided for storing the count value

of the common counter at a moment when the recovery command signal is outputted.

9. The microcomputer according to claim 1, wherein the operation clock inputted to the common counter is a sub-clock which is generated from a separated system from a main clock operating the CPU.

10. The microcomputer according to claim 9, wherein:

the microcomputer is configured in an IC; and

the sub-clock is generated by a CR oscillation circuit built in the IC.